M5W1793-02P

FLOPPY DISK FORMATTER/CONTROLLER

T-52-33-11

DESCRIPTION

The M5W1793-02P is a floppy disk formatter/controller device which accommodates single and double density formats.

The device is designed for use with microprocessors or microcomputers.

The device is fabricated with the N-channel silicon gate ED-MOS technology and is packaged in a 40-pin DIL package.

FEATURES

- Single 5V supply voltage
- TTL compatible
- Accommodate single and double density formats
  IBM 3740 single density format
  IBM system 34 double density format
- Selectable sector length (128, 256, 512 or 1024 bytes/sector)
- Side select compare
- Single/multiple sector read or write with automatic sector search
- Selectable track to track stepping time
- Write precompensation
- DMA or programmed data transfers
- Window extension

APPLICATIONS

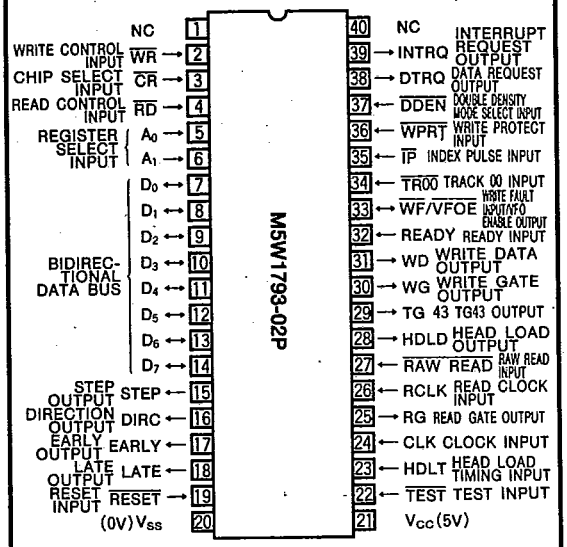
Single or double density floppy disk drive formatter/controller

8-inch or mini floppy disk interface

FUNCTION

The M5W1793-02P is a floppy disk formatter/controller that can be used with most microprocessor or microcomputer systems. The hardware of the M5W1793-02P consists of a floppy disk interface, a CPU interface and a PLA control logic. The total chip can be programmed by eleven 8-bit commands. The floppy disk interface portion performs the communication with the floppy disk drive under control of the PLA control logic. The CPU interface portion has five registers — command, data, status, track and sector register — and communicates with the CPU through the data bus. These functions are also controlled by the PLA.

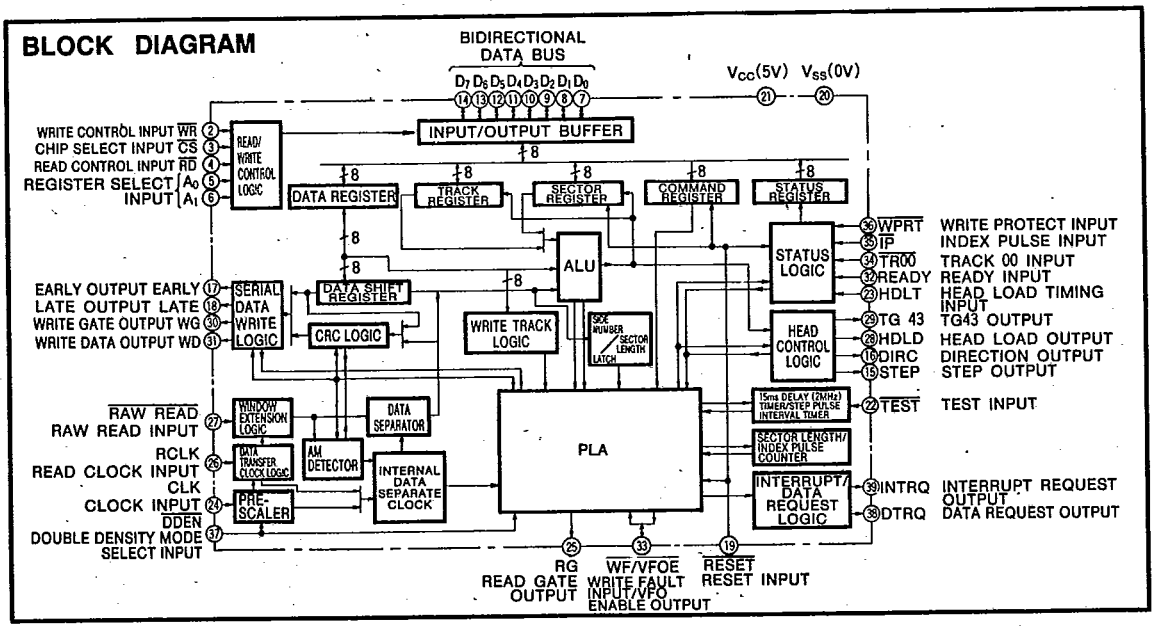
PIN CONFIGURATION (TOP VIEW)



NC: NO CONNECTION

Outline 40P4

BLOCK DIAGRAM



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PIN DESCRIPTION

Pin	Name	Input or output	Functions
NC(pin 1)	No internal connection		This pin is not internally connected.
$\overline{WR}$	Write control input	Input	Write signal from a master CPU (Active low).
$\overline{CS}$	Chip select input	Input	Chip select (Active low).
$\overline{RD}$	Read control input	Input	Read signal from a master CPU (Active low).
A_0, A_1	Register select input	Input	Register select inputs. These inputs select the register under the control of the $\overline{RD}$ and $\overline{WR}$. A_1 A_0 $\overline{RD}$ $\overline{WR}$ 0 0 STATUS REGISTER COMMAND REGISTER 0 1 TRACK REGISTER TRACK REGISTER 1 0 SECTOR REGISTER SECTOR REGISTER 1 1 DATA REGISTER DATA REGISTER
D_0~D_7	Bidirectional data bus	In/Out	Three-state, non-inverted bidirectional data bus.
STEP	Step output	Output	Step pulse output (Active high).
DIRC	Direction output	Output	Direction output. High level means the head is stepping in and low level means the head is stepping out.
EARLY	Early output	Output	This signal is used for write precompensation. It indicates that the write data pulse should be shifted early.
LATE	Late output	Output	This signal is also used for write precompensation. It indicates that the write data pulse should be shifted late.
$\overline{RESET}$	Reset input	Input	Reset input (Active low). The device is reset by this signal and automatically loads "03" (hexadecimal) into the command register. The not-ready-status bit is also reset by this signal. When reset input is made to be high, the device executes restore command even unless READY is active and the device loads "01" (hexadecimal) to the sector register.
$\overline{TEST}$	Test input	Input	This input is only used for test purposes, so user must tie it to V_{CC} or leave it open unless using voice coil actuated motors.
HDLT	Head load timing input	Input	When the device finds high level on this input, the device assumes that the head is engaged on the media. Active high.
CLK	Clock input	Input	Clock input to generate internal timing. 2MHz for 8-inch drives, 1MHz for mini drives.
RG	Read gate output	Output	This signal shows the external data separator that the syncfield is detected.
RCLK	Read clock input	Input	This signal is internally used for the data window. Phasing relation to raw read data is specified but polarity (RCLK high or low) is not important.
$\overline{RAW\ READ}$	Raw read input	Input	This input signal from the drive shall be low for each recorded flux transition.
HDLD	Head load output	Output	This output signal controls the loading of the head of the drive. The head must be loaded on the media by this high-level output.

Pin	Name	Input or output	Functions
TG43	TG 43 output	Output	This output is valid only during disk read/write operation and it shows the position of the head. High level on this output indicates that head is positioned between track 44 to 76.
WG	Write gate output	Output	This signal becomes active before disk write operations are to occur.
WD	Write data output	Output	This signal consists of data bits and clock bits. It becomes active for every flux transition. Active high.
READY	Ready input	Input	This signal shows the device the drive is ready. In the disk read/write operation except for TYPE 1 command operation, low level input terminates current operation and the device generates the INTRQ. In the TYPE 1 command operation, this signal is neglected. Not ready bit in the status register is the inverted form of this input.
$\overline{WF}/\overline{VFOE}$	Write fault input/ VFO enable output	In/Out	This is a bidirectional signal. It becomes write fault input when WG is active. In the disk write operation, low level signal on this input terminates the write operation and makes INTRQ active. This signal also appears in the status register as the write fault bit. When WG is inactive, this signal works as VFO enable output. $\overline{VFOE}$ output is also an open drain type, so pull it up to V_{CC} and never input active write fault signal when WG is inactive.
$\overline{TR00}$	Track 00 input	Input	This signal indicates that the head is located on the track 00 to the device. Active low.
$\overline{IP}$	Index pulse input	Input	This input indicates to the device that an index hole of the diskette has been encountered.
$\overline{WPRT}$	Write protect input	Input	Low level signal on this input informs the device that the drive is in the write protected state. Before disk write operations, this signal is sampled and an active low signal will terminate the current command and set INTRQ. The write protect status bit in the status register is also set.
$\overline{DDEN}$	Double density mode select input	Input	This input determines the device operation mode. When $\overline{DDEN}$=0, double density mode is selected. When $\overline{DDEN}$=1, single density mode is selected.
DTRQ	Data request output	Output	DTRQ is an open drain output, so pull up to V_{CC} by the 10k resistor. In the disk read mode, DTRQ indicates that data is assembled in the data register. In the disk write mode, it indicates that the data register is empty. DTRQ is reset by the read data or write data operation.
INTRQ	Interrupt request output	Output	INTRQ is also a open drain output, so pull up to V_{CC} by the 10k resistor. INTRQ becomes active at the completion of any command and is reset when the CPU reads the status or writes the command.
NC(pin 40)	No internal connection		This pin is not internally connected.

COMMAND DESCRIPTION

There are 11 different commands. By setting $\overline{CS}$ to "0",A_0 to "0" and A_1 to "0", the commands are written into the M5W1793-02P from the data bus at the rising edge of the $\overline{WR}$ signal.

The commands are classified into four Types : type 1, Type 2, Type 3 and Type 4.

LIST OF COMMANDS

Command type	Command	MSB			Code				LSB
Type 1 Commands	Restore command	0	0	0	0	h	V	r_1	r_0
	Seek command	0	0	0	1	h	V	r_1	r_0
	Step command	0	0	1	u	h	V	r_1	r_0
	Step-in command	0	1	0	u	h	V	r_1	r_0
	Step-out command	0	1	1	u	h	V	r_1	r_0
Type 2 Commands	Read sector command	1	0	0	m	S	E	C	0
	Write sector command	1	0	1	m	S	E	C	a_0
Type 3 Commands	Read address command	1	1	0	0	0	E	0	0
	Read track command	1	1	1	0	0	E	0	0
	Write track command	1	1	1	1	0	E	0	0
Type 4 Command	Force interrupt command	1	1	0	1	I_3	I_2	I_1	I_0

Note 1 : The M5W1793-02P features positive logic data bus and so the codes are written into the M5W1793-02P without modification.

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FLAG OPTIONS

	Flag	Description
Type 1 Commands	h : Head load flag	When h =1: The head is loaded at the beginning of the command execution. When h =0: The head is loaded when the verify operation starts if the V flag is "1". It is not loaded if the V flag is "0".
	V : Verify flag	When V =1: The contents of the track register are compared with the ID track address after head positioning. The seek error status bit is set if the desired track address is not found by the time the diskette has gone through 6 rotations. When V =0: The track verification is not performed.
	r_1, r_0 : Stepping rate flag	The stepping rate is determined by the value of these 2 bits as well as by the CLK frequency and $\overline{TEST}$ input pin.
	u : Update flag	When u = 1: The track register is updated with each step pulse: it is incremented (or decremented) by 1 for each step-in (or step-out) pulse. When u =0: Track register is not updated.
Type 2/Type3 Commands	E : 15ms delay flag(at 2MHz clock)	When E =1: Sampling of the head load timing input starts with the 15ms delay after the head load output has been set to "1". An advance is made to the next step when HDLD·HLDT = "1" is established. When E =0: Sampling of the head load timing input starts immediately after the head load output has been set to "1". An advance is made to the next step when HDLD·HLDT = "1" is established. The "next step" is the TG43 output update.
Type 2 Commands	m : Multi-sector read/write flag	When m =1: Multi-sector read/write is performed. Upon completion of one sector read/write, the sector register value is incremented by 1, the next sector is sought and read/write is performed again. Upon completion of the final sector read/write operation, the next sector is not found even when sought and so at the sixth rotation of the diskette the RNF error bit is set and the operation is concluded. This command can also be concluded with the Type 4 command. When m =0: Read/write for single sector is performed.
	S : Side select flag	When S =1: "1" is compared with the ID side number when the C flag is "1". When S =0: "0" is compared with the ID side number when the C flag is "1". No comparison is performed when C =0.
	C : Side compare flag	When C =1: The S flag and ID side number are compared. When C =0: The ID side number is not compared.
	a_0 : Data address mark flag	When a_0 = 1: The deleted data mark "F8" (hexadecimal) is written into the data field address mark. When a_0 =0: The data mark "FB" (hexadecimal) is written into the data field address mark.
Type 4 Command	I : Interrupt condition flag	When I_0 =1: The interrupt request output is set to "H" at the ready input rising edge. When I_1 =1: The interrupt request output is set to "H" at the ready input falling edge. When I_2 =1: The interrupt request output is set to "H" with the index pulse input. When I_3 =1: The command being executed is terminated and the interrupt request output is set to "H" immediately. When I_0 = I_1 = I_2 = I_3 =0: No interrupt request is generated but the command being executed is terminated. This command is executed so that the interrupt request output, which has been set by the Type 4 command, is reset by the following command write or status read.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5~7	V
V_I	Input voltage		−0.5~7	V
V_O	Output voltage		−0.5~7	V
P_d	Power dissipation	T_a=25℃	350	mW
T_{opr}	Operating free-air temperature range		0~70	℃
T_{stg}	Storage temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=0~70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V

ELECTRICAL CHARACTERISTICS (T_a=0~70℃, V_{CC}=5V±5%, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage		V_{SS}−0.5		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−200μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL}=1.8mA			0.45	V
I_{CC}	Supply current				70	mA
I_I	Input current.(HDLT, $\overline{TEST}$, $\overline{WF/VFOE}$, $\overline{WPRT}$, $\overline{DDEN}$)	V_I=V_{CC}~0V	−100		10	μA
	Input current other inputs	V_I=V_{CC}~0V	−2.5		2.5	
I_{OZ}	Off-state output current	V_I=V_{CC}~0V	−10		10	μA

TIMING REQUIREMENTS (T_a=0~70℃, V_{CC}=5V±5%, V_{SS}=0V, unlese otherwise noted)

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{su(A-R)}$ $t_{su(CS-R)}$	Address and chip select setup time before read	TSET		50			ns
$t_{h(R-A)}$ $t_{h(R-CS)}$	Address and chip select hold time after read	THLD		10			ns
$t_{w(R)}$	Read pulse width	TRE	C_L=50pF	280			ns
$t_{su(A-W)}$ $t_{su(CS-W)}$	Address and chip select setup time before write	TSET		50			ns
$t_{h(W-A)}$ $t_{h(W-CS)}$	Address and chip select hold time after write	THLD		10			ns
$t_{w(W)}$	Write pulse width	TWE		200			ns
$t_{su(DQ-W)}$	Data setup time before write	TDS		250			ns
$t_{h(W-DQ)}$	Data hold time after write	TDH		20			ns
$t_{w(\overline{RR})}$	Raw read pulse width	T_{PW}	(Note1, 2)	100	200	250	ns
$t_{C(\overline{RR})}$	Raw read cycle time	Tbc	(Note 3)	1600	2000		ns
$t_{w(RCLK)}$	Read clock high-level width	Ta	(Note 4)	800			ns
$t_{w(\overline{RCLK})}$	Read clock low-level width	Tb	(Note 4)	800			ns
$t_{C(RCLK)}$	Read clock cycle time	Tc		1600			ns
$t_{h(RCLK-\overline{RR})}$	Read clock hold time before raw read	T_{x1}		40			ns
$t_{h(\overline{RR}-RCLK)}$	Read clock hold time after raw read	T_{x2}	FM	40			ns
			MFM	40			
$t_{w(WD)}$	Write data pulse width	Twp	FM	450	500	550	ns
			MFM	150	200	250	
$t_{C(WD)}$	Write data cycle time	Tbc	(Note 5)		2, 3, 4		μs
$t_{w(\phi)}$	Clock high-level pulse width	TCD_1		230	250	20000	ns
$t_{w(\overline{\phi})}$	Clock low-level pulse width	TCD_2		200	250	20000	ns
$t_{w(RESET)}$	Reset pulse width	TMR		50			μs
$t_{w(IP)}$	Index pulse width	TIP	(Note 5)	10			μs
$t_{w(WF)}$	Write fault pulse width	TWF	(Note 5)	10			μs

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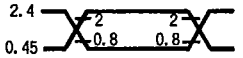
SWITCHING CHARACTERISTICS (T_a=0~70℃, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{PLH(WG-WD)}$	Propagation time from write gate to write data	Twg	FM (Note 5)		2		μs
			MFM (Note 5)		1		
$t_{PLH(E-WD)}$ $t_{PLH(L-WD)}$	Propagation time from early or late to write data	Ts	MFM (Note 5)	125			ns
$t_{PHL(WD-E)}$ $t_{PHL(WD-L)}$	Propagation time from write data to early or late	Th	MFM (Note 5)	125			ns
$t_{PHL(WD-WG)}$	Propagation time from write data to write gate	Twf	FM (Note 5)		2		μs
			MFM (Note 5)		1		
$t_{PZV(R-DQ)}$	Output enable time after read	TDACC	C_L=50pF			250	ns
$t_{PVZ(R-DQ)}$	Output disable time after read	TDOH	C_L=50pF	50		150	ns
$t_{PHL(R-DRQ)}$	Propagation time from read to DRQ	TDRR(RD)				250	ns
$t_{PHL(R-INTRQ)}$	Propagation time from read to INTRQ	TIRR(RD)	(Note 5)			500	ns
$t_{PHL(W-DRQ)}$	Propagation time from write to DRQ	DRR(WR)				250	ns
$t_{PHL(W-INTRQ)}$	Propagation time from write to INTRQ	TIRR(WR)	(Note 5)			500	ns
$t_{W(STP)}$	Step pulse width	TSTP	(Note 5)	2or4			μs
$t_{PLH(DIR-STP)}$	Propagation time from direction to step	TDIR	(Note 5)	12			μs
$t_{V(WD-CLK)}$	Write data valid time before clock	Twd1	CLK=1MHz MFM	200			ns
			CLK=2MHz MFM	30			
$t_{V(CLK-WD)}$	Write data valid time after clock	Twd2	CLK=1MHz MFM	50			ns
			CLK=2MHz MFM	50			

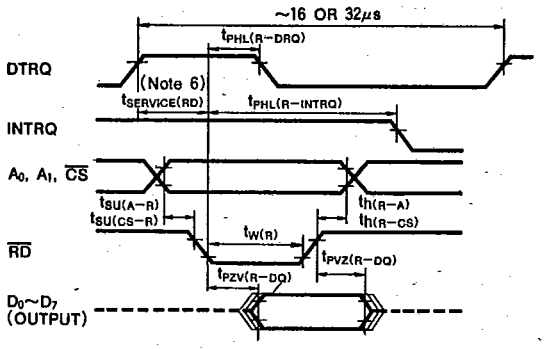
Note 1 : The pulse of $\overline{\text{RAW READ}}$ may be any width if pulse is entirely within RCLK. When the pulse occurs in the RCLK window, $\overline{\text{RAW READ}}$ pulse width must be less than 300 ns for MFM mode and 600 ns for FM mode at CLK=2MHz. Times double for 1MHz.
2 : 100 ns pulse width is recommended for the $\overline{\text{RAW READ}}$ pulse in 8 MFM mode.
3 : $\overline{\text{RAW READ}}$ cycle time $T_{C(RR)}$ and WD cycle time $T_{C(WD)}$ is normally 2μs in MFM and 4μs in FM. Times double when CLK=1MHz.
4 : The polarity of RCLK during $\overline{\text{RAW READ}}$ is not important.
5 : Times double when CLK=1MHz.
6 : A. C Testing waveform

Input pulse level	0.45~2.4V
Input pulse rise time	20ns
Input pulse fall time	20ns
Reference level input	V_{IH}=2V, V_{IL}=0.8V
output	V_{OH}=2V, V_{OL}=0.8V

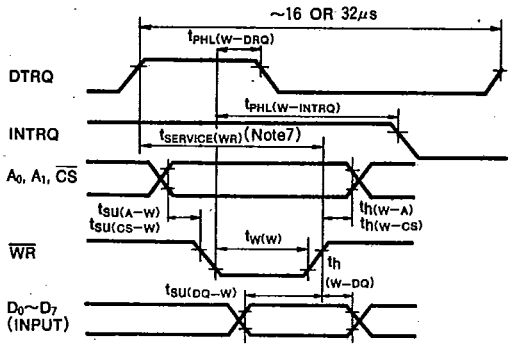


TIMING DIAGRAM

Read

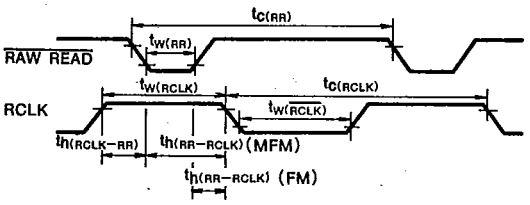


Write

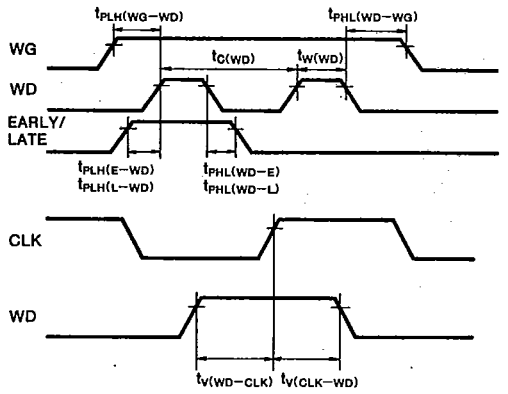


Note 7 : $t_{SERVICE(RD)}$ maximum value, FM: 27.5μs, MFN: 13.5μs
8 : $t_{SERVICE(WR)}$ maximum value; FM: 23.5μs, MFM: 11.5μs

Read data



Write data



Others